AMENDED CLAIMS

[received by the International Bureau on 8 April 2005 (08.04.2005);
original claims 1, 2, and 4 amended;
remaining claims unchanged (2 pages)]

1. A method of forming a lattice-tuning semiconductor substrate, comprising:

(a) defining a selected area (12) of a semiconductor surface (15) by means of a window (13) extending through an isolating layer (11) on the semiconductor surface (15);

(b) defining in the vicinity of the window (13) a depression (14) in the isolating layer (11);

(c) growing on top of the selected area (12) of the semiconductor surface (15) an active layer (16) of a semiconducting material that is not lattice-matched to the material of the semiconductor surface (15) such that dislocations (17) are formed in the window (13) to relieve the strain in the active layer (16); and

(d) further growing the active layer (16) to overgrow the isolating layer (11) and fill the depression (14) to form a substantially dislocation-free area (18) of said semiconducting material within the depression (14).

2. A method according to claim 1, wherein, after the growing of the active layer (16) to fill the depression (14), the portion of the active layer (16) that has overgrown the isolating layer (11) is removed so as to isolate the substantially dislocation-free area (18) of said semiconducting material within the depression (14) from the area of said semiconducting material within the window (13).

3. A method according to claim 2, wherein the portion of the active layer (16) that has overgrown the isolating layer (11) is removed by polishing down to the level of the isolating layer (11).

4. A method according to claim 1, 2 or 3, wherein, after the growing of the active layer (16) to fill the depression (14), the active layer (16) and the isolating layer (11) are removed from the semiconductor surface (15) except in the vicinity of the depression (14) so as to leave on the semiconductor surface (15) the substantially dislocation-free area (18) of said semiconducting material isolated from the semiconductor surface (15) by the portion of the isolating layer (11).

5. A method according to claim 4, wherein the active layer (16) and the isolating layer (11) are removed from the semiconductor surface (15) by etching.

6. A method according to any preceding claim, wherein the active layer (16) is annealed at an elevated temperature in order to substantially fully relieve the strain in the active layer (16).

7. A method according to claim 6, wherein the growth of the active layer (16) is carried out at a temperature in the range from room temperature to 1200°C, and preferably in the range from 350 to 900°C, and the annealing of the active layer (16) is carried out at an elevated temperature in the range from room temperature to 1500°C, and preferably in the range from 500 to 1200°C.

8. A method according to any preceding claim, wherein the semiconductor surface is a Si surface, and the semiconducting material of the active layer (16) is SiGe.

9. A method according to claim 8, wherein the active layer (16) has a Ge composition ratio that is substantially constant within the SiGe layer (16).

10. A method according to claim 8, wherein the active layer (16) comprises first and second sub-layers, one of the sub-layers having a Ge composition ratio that is substantially constant within the sub-layer, and the other sub-layer having a Ge composition ratio that increases within the layer from a first level to a second level greater than the first level.